

THURSDAY OCTOBER 25

OPENING SESSION (Thursday 4-5pm)

Welcoming Remarks

General Chair – Yervant Zorian, Virage Logic

Program Chair – Andrew B. Kahng, UC San Diego

Plenary Talk P.1. *The IMPACT Research Program at the University of California – Addressing DFM&Y at 22nm*

Prof. Kameshwar Poolla, UC Berkeley

Plenary Talk P.2. *New DFM Wave to Overcome Variability Crisis in Sub-45nm Technology nodes*

Prof. Andrzej Strojwas, PDF Solutions and CMU

SESSION 1: Connecting Test & Diagnosis to Yield Optimization (Thursday 5-7pm)

1.1 *On the Correlation between Yield and DFM through Diagnosis*

M. Sonza Reorda, P. Bernardi, F. Melchiori, R. Sirtori, V. Tancorre, and D. Appello, Politecnico di Torino and STMicroelectronics, Italy

1.2 *Bridging Test, Diagnosis and DFM*

Anne Gattiker, IBM Corporation

1.3 *Yield Acceleration based on Programmable Test & Diagnosis*

Y. Zorian, G. Torjyan, D. Nenni, H. Nalbandian, Virage Logic

1.4 *Mixed Test Structure for Soft and Hard Defect Detection*

Jean-Michael Portal, Laboratoire Materiaux et Microelectronique

1.5 *A Built-In Self-Repair for NAND Flash Memory*

Yu-Ying Hsiao and Cheng-Wen Wu, National Tsing Hua University

1.6 *A Redesign Technique to Improve Manufacturing Yield by Exploiting Error Tolerance*

Doochul Shin and Sandeep K. Gupta, University of Southern California

EVENING RECEPTION (Thursday 7-9pm)

FRIDAY OCTOBER 26

SESSION 2: PHYSICAL DESIGN AND MANUFACTURABILITY VERIFICATION (Friday 8-10am)

2.1 DFM Optimization of Standard Cells Core Libraries
Fabio Melchiori and Roberto Sirtori, STMicroelectronics

2.2 Regularity-Enhanced Layout of Standard Cells
Hidetoshi Onodera and Hiroaki Muta, Kyoto University

2.3 VariTamer: A Heterogeneous Platform for Deciding the Best Layout Placement in Physical Implementation
Jwu-E Chen, H.W. Huang, C.Y. Ho, and H.C. Liang, National Central University and Chung Yuan Christian University, Taiwan

2.4 Via-Configurable Transistor Array: A Regular Design Technique to Improve ICs Yield
Marc Pons, Francesc Moll, Antonio Rubio, Jaume Abella, Xavier Vera and Antonio Gonzalez Universitat Politecnica de Catalunya and Intel Barcelona

2.5 Flexible Model-Based DRC and DFM Verification
Fedor G. Pikus, Mentor Graphics, Inc.

SESSION 3 (INVITED): DFM&Y FUTURES FOR EDA (Friday 10:30am-12noon)

3.1 Physical Signoff -- Bringing DFM Signoff into the Flow
John Lee, Magma Design Automation

3.2 DFM: From Buzz to Norm
Joe Sawicki, Mentor Graphics

3.3 How to Push Polygons to the Limit and Still Yield
Dipu Pramanik, Cadence Design Systems

SESSION 4: VARIABILITY AND YIELD (Friday 1pm – 3pm)

4.1 A Designer's Approach to Modeling Process Variability
Dejan Markovic, UCLA EE Department

4.2 DFM Technology Roadmap Including Dimensional Variability
Juan Antonio Carballo, Praveen Elakkumanan, and Sani Nassif, Argon Venture Partners, IBM East Fishkill, and IBM Austin Research Laboratory

4.3 A Systematic Variation Aware Circuit Simulation Engine
Shayak Banerjee, Praveen Elakkumanan, Duresti Chidambarrao, James Culp, Saibal Mukhopadhyay, and Michael Orshansky, University of Texas at Austin and IBM East Fishkill

4.4 Statistics and Digital Design: Exploiting the Corners

Kambiz Samadi, Mark Nakamoto, and Riko Radojcic, UC San Diego and Qualcomm CDMA Technologies

4.5 Non-Gaussian Statistical Timing Analysis Using Second-Order Polynomial Fittings
Lerong Cheng, Jinjun Xiong, and Lei He, UCLA and IBM Research

4.6 On the Opportunity to Improve System Yield with Multi-Core Architectures
Yury Markovsky and John Wawrzynek, University of California, Berkeley

PANEL: From David to Goliath: The Role of Startups in the Evolution of DFM (Friday 3-5pm)

Organizer/Moderator:

- Juan-Antonio Carballo, Argon Venture Partners

Panelists:

- Bob Gleason, Luminescent
- Ara Markosian, Ponte Solutions
- Frank Schellenberg, Mentor Graphics
- Atul Sharan, Cadence
- Clive Wu, Blaze DFM