5th IEEE International Workshop on
Design for Manufacturability & Yield (DFM&Y 2011)
San Diego Convention Center, San Diego, California, USA
June 6, 2011

Co-located with the 48th Design Automation Conference

Call for Papers

Scope: Increased manufacturing variability in leading-edge process technologies requires new paradigms and solution technologies for yield optimization. SoC manufacturability and yield entails design-specific optimization of the manufacturing, and thus enhanced communications across the design-manufacturing interface. A wide range of Design-for-Manufacturability (DFM) and Design-for-Yield (DFY) methodologies and tools has been proposed in recent years. Some of these tools are leveraged during back-end design, others are applied just before manufacturing handoff, and still others are applied post-design, from reticle enhancement and lithography through wafer sort, packaging, final test and failure analysis. DFM and DFY can dramatically impact the business performance of chip manufacturers. It can also significantly affect age-old chip design flows. Using DFM and DFY solutions is an investment, and choosing the most cost effective one(s) requires careful analysis of integration and schedule overheads, versus quantified benefits. This workshop analyzes this key trend and its challenges, and provides an opportunity to discuss a range of DFM and DFY solutions for today’s SoC designs.

Representative topics include, but are not limited to:

- Electrical, Design-Driven DFM
- Built-in Repair Analysis and Self-Repair
- Adaptive Design Techniques in DFM/DFY
- Embedded Test and Diagnosis
- OPC and RET
- DFM for 3D Integration
- DFM at System/Architecture Level
- Analog and Mixed-Signal DFM
- Process Monitoring IP
- Statistical Design
- Test-based Yield Learning
- Design-Aware Manufacturing
- Yield Enhancement IP
- Yield Management

Information for Authors

To present at the Workshop, authors are invited to submit unpublished extended abstracts or full papers, 2 to 4 pages in length. Submissions on ambitious works in progress are also encouraged. Each submission should include a short abstract of 50 words, and keywords. The review process is blind. Please do not include author names or affiliations. Proposals for embedded tutorials and panel discussions are also invited.

Submit a copy of your paper proposal as a PDF at http://www.easychair.org/conferences/?conf=dfmy2011

The goal of the workshop is to foster unrestricted discussion in the field of design-manufacturing interactions. Copies of papers will be provided to attendees in the form of Workshop Notes, but no proceedings will be published. Therefore, accepted papers can still be submitted to other conferences and journals.

Submissions are due no later than April 10th, 2011.

Authors will be notified of the disposition of their papers by April 25th, 2011.

Authors of accepted papers must submit an illustrated text by May 15th, 2011 for inclusion in the Workshop Notes, which will be provided to the attendees.

DFM&Y 2011 is sponsored by the IEEE Computer Society Test Technology Technical Council (TTTC) in cooperation with the IEEE Council on Electronic Design Automation (CEDA). For more information on DFM&Y 2011, visit the workshop website at: http://vlsicad.ucsd.edu/DFMY