# Design for Manufacturability and Yield 2013 (DFM&Y)

Date: Monday, June 3, 2013  
Location: Austin Convention Center (Room 18AB), Austin, Texas, USA  
(Co-located with 50th ACM/EDAC/IEEE Design Automation Conference, June 2-6, 2013)

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<th>Start</th>
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<td>8:45 AM</td>
<td>8:50 AM</td>
<td>Welcome and opening remarks</td>
<td>Will Conley</td>
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<td>Design for Yield - Chair: Rasit Topaloglu (IBM-USA)</td>
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| 8:50 AM        | 9:30 AM      | Keynote: Smart Statistical Methodology: A Crystal Ball for Robust      | Rajiv Joshi  
IBM TJ Watson Research Ctr, Yorktown Heights NY (USA) |
|                |              | Design Model using a Lithography Hotspot Classifier                   | Sergio Gomez Fernandez  
Universitat Politecnica de Catalunya - Barcelona (Spain)               |
| 9:55 AM        | 10:20 AM     | Addressable array for full transistor characterization and yield       | David Ouyang  
Semiconductors Corporation (China)                                       |
| 10:20 AM       | 10:35 AM     | Break                                                                |                                                                        |
|                |              | Design for Mfg - Chair: Juan Rey (Mentor Graphics-USA)                |                                                                        |
| 10:35 AM       | 11:00 AM     | A Study of Robust Stitch Design for Litho Etch Double Patterning      | Yoko Takekawa  
Toshiba Semiconductor & Storage Products, Japan                        |
| 11:00 AM       | 11:25 AM     | Design for Manufacturability and Reliability in TSV-based 3D-IC       | David Pan  
University of Texas at Austin, USA                                     |
| 11:25 AM       | 11:50 AM     | Role of E-Beam Inspection for Integrated Circuit Design for           | Rasit O Topaloglu  
IBM Corp, East Fishkill, NY, USA                                         |
| 11:50 AM       | 12:15 PM     | Dealing with On chip and Off chip variations for high speed           | Arvind NV, Siva Kothamasu, Snehamay Sinha  
Texas Instruments, Dallas, Texas USA                                     |
|                |              | Break                                                                |                                                                        |
|                |              | DFM for Multiple Patterning - Chair: Arjun Rajagopal (TI-USA)         |                                                                        |
| 12:15:00 PM    | 12:45 PM     | Triple-Patterning and SADP: Technology and Physical Design Implications | Kevin Lucas  
Synopsys, Austin, Texas, USA                                             |
| 12:45 PM       | 1:10 PM      | Minimum Cost Stitch Selection in LELE Double Patterning               | Yukihide Kohira  
The University of Aizu (Japan)                                           |
|                |              | DFM & Y Panel Chair: Andrew Kahng                                     |                                                                        |
| 1:10-2:20 PM   |              | Panel discussion-Chair: Andrew Kahng                                  | “The Technology Roadmap for DFM”  
Patrick Groeneveld, Synopsys  
Greg Yeric, ARM  
Jim Culp, IBM  
Puneet Sharma, Freescale  
Vassilios Gerousis, Cadence  
Riko Radojcic, Qualcomm                                                   |
| 2:20 pm        | 2:45 PM      | Logic Synthesis for Manufacturability Considering Regularity and       | Lucas Machado  
UFRGS (Federal University of Rio Grande do Sul)  
Brazil                                                               |
|                |              | Lithography Printability                                              |                                                                        |
| 2:45 PM        | 3:00 PM      | Break                                                                |                                                                        |
|                |              | Session Name -Variability - Chair: Mohamed Allam (Qualcomm-USA)      |                                                                        |
| 3:00 PM        | 3:25 PM      | Statistical Diagnosis for Systematic Defects Based on Physical        | Po-Juei Chen  
Taiwan National Taiwan University, Taiwan                                  |
|                |              | Features                                                              |                                                                        |
| 3:25 PM        | 3:50 PM      | Variability-aware SRAM design                                         | Mohamed Abu-Rahma  
Qualcomm, San Diego, CA USA                                                |
| 3:50 PM        | 4:15 PM      | Open DFM and OPEX for DRC and DFM                                     | Jake Buurma, S2, USA                                                     |
| 4:15 PM        | 4:40 PM      | Design Technology Co-optimization Framework for early evaluation of  | Arindam Mallik  
IMEC. Leuven, Belgium                                                      |
|                |              | FinFET-based Advanced Technology Nodes                                |                                                                        |
| 4:40 PM        | 4:45 PM      | Closing Remarks                                                       | Will Conley                                                             |